

## REMARKS

### Summary

In this Office Action, claims 1-5 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,476,498 issued to Marathe (hereinafter "*Marathe*") in view of U.S. Patent 5,592,024 issued to Aoyama et al. (hereinafter "*Aoyama*") or U.S. Patent 6,806,184 issued to Chen et al. (hereinafter "*Chen*"). Additionally, claims 5-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Marathe* taken with *Aoyama* or *Chen*, and further in view of U.S. Patent Application Publication 2002/0024150 of Farrar (hereinafter "*Farrar*"). Further, claims 21-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Marathe* taken with *Aoyama* or *Chen*, and further in view of *Farrar* and U.S. Patent Application Publication 2002/0184490 of McCown et al. (hereinafter "*McCown*").

Thus, claims 1-8 and 21-24 currently are pending.

In response, claims 1 and 21 have been amended, without departing from the scope of the original disclosure and without introducing new matter, placing said claims and claims 2-8 and 22-24 which depend therefrom, in condition of allowance.

### Claim Rejections under 35 U.S.C. § 103(a)

#### 1. Claims 1-5 and 8: *Marathe/Aoyama* or *Chen*

Claims 1-5 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Marathe* in view of *Aoyama* or *Chen*. In response, claim 1 has been amended, placing said claim, and claims 2-5 and 8 which depend therefrom, in condition of allowance.

Independent claim 1, as amended, is directed to a semiconductor device comprising, among other things:

a damascene interconnect structure defined in the dielectric layer, the damascene interconnect structure having a bottom portion isolated from a conductive channel disposed on a bottom surface of the dielectric layer; and

a barrier layer deposited within the damascene interconnect structure, the barrier layer within the damascene interconnect structure having a tapered profile adapted to resist overhang formation and achieve at least substantially complete gap-filling of the damascene interconnect structure.

Thus, when viewed in whole, the invention as claimed discloses a novel structural combination improving gap fill of damascene interconnect structures.

In contrast, *Marathe* fails to teach, disclose, or suggest the damascene interconnect structure as claimed in claim 1. Rather, *Marathe* discloses a damascene interconnect structure **206** interfacing a conductive channel **230** disposed on the bottom surface of a dielectric layer **212** in which the damascene interconnect structure **206** is disposed. *Marathe* disclosure is directed to avoiding void nucleation at those very locations (i.e., the interfaces of the damascene interconnect structure with the conductive channel), and in fact discloses that other locations have normal barrier-layer thicknesses (i.e., conformal barrier layers). See *Marathe*, Fig. 3; 5:57-60 (“the barrier **232** is optimized by increasing the thickness of the bottom **231** over the first channel **202** and the thickness of the sides **233** on the sidewalls of the via dielectric **212** over the thickness outside of the via **206**,” emphasis added). Thus, *Marathe* cannot be said to teach, disclose, or suggest a damascene interconnect structure having a bottom portion isolated from a conductive channel disposed on the bottom surface of the dielectric layer.

Regarding this point, Examiner suggested that there is no support in Applicants’ Specification for the limitation regarding the damascene interconnect structure not being coupled to a conductive channel, as previously amended. See *Office Action*, p.6, lines 10-11. However, Applicants respectfully disagree. Applicants direct Examiner to Figure 8 which clearly shows a damascene interconnect structure **120** not coupled or

interfacing a conductive channel. Thus, Applicants respectfully assert that the invention as claimed is in fact supported by the disclosure.

Examiner also suggested that the foregoing limitation is not in accord with language in the Specification stating that the dielectric layer **104** may be on a metallization stack. See *Office Action*, p. 6, lines 11-13 (citing Specification, para. 18, 19). However, the recited passage from Applicants' Specification cannot be read to mean the claimed damascene interconnect structure may in fact interface a conductive channel because the recited passage merely discusses the dielectric layer being over a metallization stack. As the drawings and the claims teach, the damascene interconnect structure may be isolated from a conductive channel disposed on a bottom surface of the dielectric layer. Thus, if a conductive channel were disposed on a bottom surface of the dielectric layer, the damascene interconnect structure may have a configuration as shown in Figure 8 wherein the damascene interconnect structure is not formed through the entire width of the dielectric layer. Thus, Applicants respectfully assert that the invention as claimed is in fact supported by the Specification.

However, even if *Marathe* could be said to disclose a damascene interconnect structure having a bottom portion isolated from a conductive channel disposed on the bottom surface of the dielectric layer, *Marathe* cannot be said to teach, disclose, or suggest a barrier layer within the damascene interconnect structure having a tapered profile adapted to resist overhang formation and achieve at least substantially complete gap-filling of the damascene interconnect structure. Examiner suggested that *Marathe* discloses a damascene interconnect structure having a tapered profile. See *Office Action*, p. 3 (citing *Marathe*, 6:60-68, Fig. 3). However, Applicants respectfully disagree because *Marathe* simply discusses the use of a barrier layer **232** wherein the bottom and sidewalls are thicker than those areas outside of the damascene interconnect structure **206** to avoid void nucleation at via-channel interfaces. Even if *Marathe's* Figure 3 could be said to disclose a damascene interconnect structure having a tapered profile, Applicants fail to see any teaching in *Marathe* of a barrier layer adapted to resist overhang formation and achieve substantially complete gap-filling of the damascene

interconnect structure. Rather, *Marathe*'s damascene interconnect structure is directed simply to a damascene interconnect structure adapted to avoid void nucleation at via-conductive channel interfaces. Thus, *Marathe* cannot be said to teach, disclose, or suggest each and every limitation of the invention as claimed in claim 1.

Furthermore, there is no suggestion in *Marathe*, *Aoyama*, or *Chen* to combine their respective teachings to arrive at the claimed invention. *Marathe* discloses a solution to via-conductive channel void nucleation. Although *Aoyama* and *Chen* disclose interconnect structures having bottom portions not interfacing a conductive channel, one skilled in the art would not be motivated to use damascene interconnect structures having thicker bottoms and sidewalls (or tapered, as the Examiner suggested) because one skilled in the art would not have the requisite desire to combine the references. To do so would involve added process steps and materials, leading to increased processing costs and time. Furthermore, *Marathe* teaches explicitly that its barrier layer is thicker at via-channel interfaces than in other damascene structures. Put another way, one skilled in the art would simply be led to using *Marathe*'s damascene interconnect structures only where needed, i.e., at via-conductive channel interfaces, and conformal barrier layers in other locations.

Therefore, *Marathe*, *Aoyama*, and *Chen*, whether alone or combined, cannot be said to teach, disclose, or suggest the novel structural combination improving gap fill as claimed in claim 1.

Accordingly, claim 1 stands patentable over *Marathe*, *Aoyama*, and *Chen*. Further, dependent claims 2-5 and 8 depend from claim 1 and therefore also are patentable over *Marathe*, *Aoyama*, and *Chen*.

2. Claims 5-8: *Marathe/Aoyama* or *Chen/Farrar*

Claims 5-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Marathe* taken with *Aoyama* or *Chen*, and further in view of *Farrar*. Applicants respectfully traverse. *Farrar* does not remedy the above-discussed deficiencies of

*Marathe*, *Aoyama*, and *Chen*, and thus, for at least the same reasons, claim 1 remains patentable over *Marathe*, *Aoyama*, and *Chen* even when combined with *Farrar*.

Claims 5-8 depend from claim 1 thereby incorporating the limitations of claim 1. Therefore, claims 5-8 are patentable *Marathe*, *Aoyama*, *Chen*, and *Farrar* combined.

3. Claims 21-24: *Marathe/Aoyama or Chen/Farrar/McCown*

Claims 21-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Marathe* taken with *Aoyama* or *Chen*, and further in view of *Farrar* and *McCown*. Applicants respectfully traverse. Independent claim 21 includes the same limitations as those of claim 1 and thus, for at least the same reasons discussed above, Applicants respectfully submit that claim 21 also is patentable over *Marathe*, *Aoyama*, *Chen*, and *Farrar*. *McCown* does not remedy the above-discussed deficiencies of those references and thus, for at least the same reasons, claim 21 is patentable over those references, even when combined with *McCown*.

Claims 22-24 depend from claim 21 thereby incorporating the limitations of claim 21. Therefore, claims 21-24 are patentable over *Marathe*, *Aoyama*, *Chen*, *Farrar*, and *McCown* combined.

## CONCLUSION

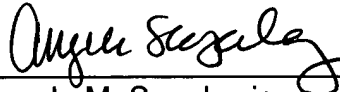
In view of the foregoing, Applicants respectfully submit that claims 1-8 and 21-24 are in condition of allowance. Thus, entry of the offered amendments and early issuance of Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,  
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: \_\_\_\_\_

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Angela M. Sagalewicz  
Registration No. 56,113

Pacwest Center, Suite 1900  
1211 SW Fifth Avenue  
Portland, Oregon 97204  
Telephone: 503-796-3756